Design of Ka-band Frequency Source Based on PLL

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Abstract. In communication，radar and electronic measuring instruments and other fields, the high demanding of frequency source need wider band, lower phase noise and spurs, and small frequency step. In order to meet the demand of system calibration，a low phase noise and spurs, small frequency step frequency source is developed. The advantages and disadvantages of various frequency source signals are analyzed, using the phase discriminator(PD:HMC704) and the voltage controlled oscillator(VCO:HMC531) of ADI Company and optimal design, a ka-band Frequency Source is designed successfully, a sign is output based PLL, frequency multiplication and filter, the phase noise are simulated，and the factors affecting the spurious dispersion and the solutions are discussed. The test results show that the output frequency range of the frequency source is 26～28.4GHz, the phase noise is -86.05dBc / Hz@10kHz，step-by-step is 1MHz，which achieves a higher level than similar products.

Keywords: frequency source; small step; PLL; frequency multiplication; filter.

1. Introduction

Frequency source (also known as signal source) is an important part of modern electronic system, which has been widely applied to such fields as aerospace and communication.[1] At present, high requirements are put forward for its small step ,high frequency and low phase noise and other indexes. It can be used as both interference signal generator and standard signal source.[2] However, the above indexes restrict each other, and how to choose the appropriate frequency synthesis scheme to achieve the optimal overall performance has become a difficult problem in engineering design.[3] In order to solve this problem, the technicians have designed high performance frequency sources using frequency synthesis technology, that is, one or more reference frequencies are processed by circuit mixing, frequency doubling or frequency division in order to produce one or more required frequencies.[4]

In this paper, the idea of frequency source design based on phase-locked loop technology is proposed to achieve single carrier frequency output in Ka-band, which has the characteristics of low phase noise and high capacity of suppressing stray signals.

2. Beacon machine principle

2.1 Composition and Principle

Beacon machine is a device composed of RF circuit, control circuit and power supply circuit, which can complete the transmission of single carrier signal, and is used for automatic phase calibration of the trio-system of antenna, servo and feed, directional sensitivity calibration, G/T value measurement, channel delay test, gain consistency calibration and other calibration work[5]. It mainly includes: voltage regulator module , microcontroller and phase-locked loop circuit, interface circuit and so on.[6] Its voltage regulator module stabilizes the output voltage of the power supply into the voltage required by the phase detector, VCO and other devices.[7] The master computer completes the on-off control of the beacon machine, the frequency setting of the output signal, the level setting

of the output signal, the left-turn and right-turn output switch, and the state of the receiving the beacon machine.

The realization of frequency source mainly includes three ways: direct frequency synthesis, direct digital frequency synthesis (DDS) and indirect (phase-locked) frequency synthesis.[8] The advantages of direct frequency synthesis are fast frequency hopping speed and low phase noise, but its disadvantages are large size and high cost.[9] The advantages of direct digital frequency synthesis are fast frequency hopping speed and high frequency resolution, but the disadvantages are low frequency accuracy and high spur.[10] The advantages of indirect frequency synthesis are wide output frequency range, low spurious and simple circuit, but the disadvantage is slow frequency hopping speed[11].

The schematic diagram of beacon unit is shown in Figure 1.

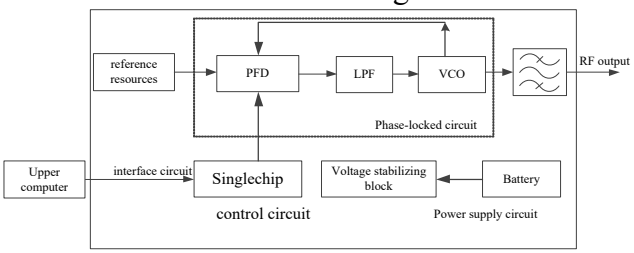

Figure 1 The schematic diagram of beacon unit

2.2 Technical Specifications

Output frequency: 26.0GHz～28.35GHz，1MHz step;

Output level : ≥0dBm (when the output attenuation value is minimum);

Output level adjustable range: ≥60dB，2dB step;

Frequency accuracy: better than 2×10-6;

Frequency Short-term stability: better than 1×10-9/s;

The phase noise of the highest output frequency of the beacon machine shall not exceed the following range;

–70dBc/Hz@1kHz offset

–75dBc/Hz@10kHz offset

With the left-turn and right-turn output switch which can be switched to select output.

3. Beacon machine design

3.1 Circuit Principle

The beacon machine adopts 100MHz clock signal as the reference clock of the frequency synthesizer, and generates 13G~ 14.2GHz signal through PLL ring. After filtering, amplification and frequency doubling, it outputs is 26G- 28.35GHz signal with a step of 1MHz. The principle diagram is shown in FIG.2.

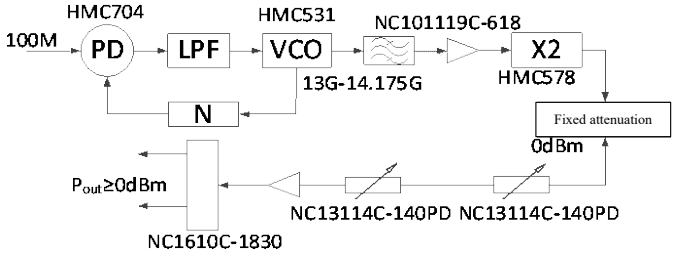

Figure 2 The schematic diagram of beacon unit

As shown in the figure above, the first stage amplifier adopts NC101119C chip, which is a low P-1 amplifier and P-1 is about 7dBm. In order to ensure high frequency and undistorted amplification of the signal, this stage amplifier works in a shallow saturation state.

Two attenuators with NC13114-140 chips are set at the rear stage of the beacon link, which can meet the dynamic requirements of 60dB dynamic range and step 2dB and finally through the control of the switch, it can realize two signals output.

3.2 Main Chips

In order to meet the index requirements of low phase noise, low spur , the chip with low noise performance is selected on the basis of ensuring frequency accuracy. In this paper, HMC704 chip is adopted for phase detector, HMC531 is adopted for VCO, and AD797 chip is adopted for low noise operational amplifier.

Among them, HMC704 chip is a PLL with the function of 8GHZ RF input and 19-bit prescaler, which has the leading phase noise and spur suppression performance. It adopts SPI bus to control the pre-frequency divider R and frequency divider N to achieve precise voltage output. Its circuit principle is shown in Figure 3.

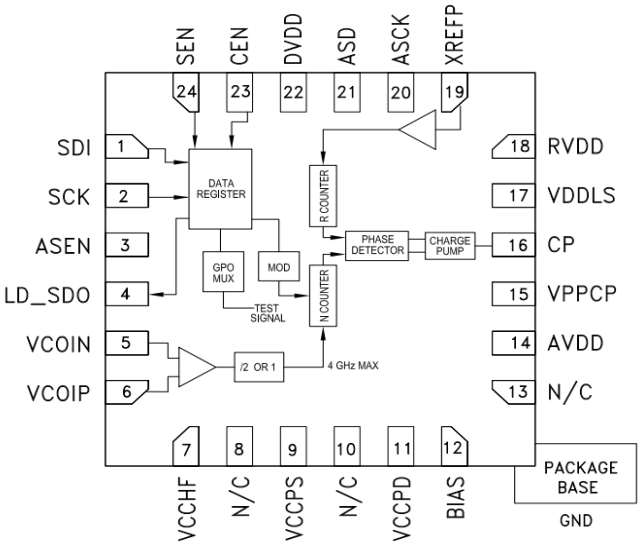

Figure 3 Schematic diagram of HMC704

HMC531 chip has the characteristics of wide frequency band and low phase noise, and comes with 1/2 and 1/4 frequency division ports .Its frequency output range can cover 13G~14. 2GHz, step 0.5MHz. The phase noise can reach -110dBc /Hz at 100kHz, and its circuit schematic is shown in Figure 4.

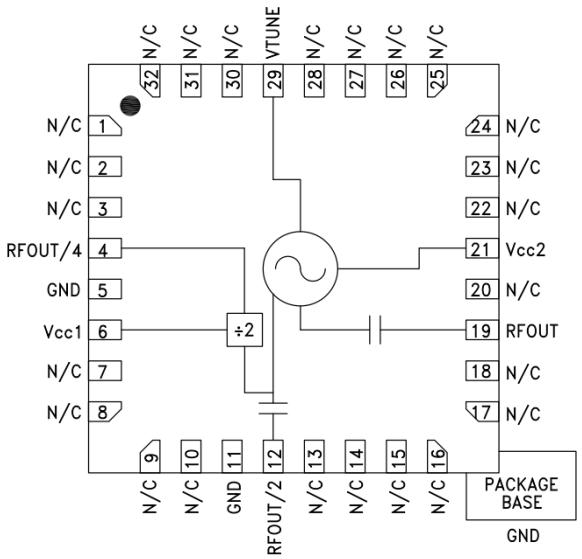

Figure 4 Schematic diagram of HMC531

The amplifier at the rear of PLL uses AD797chip,which can realize loop filter so as to reduce the deterioration of the phase noise caused by the operational amplifier.

3.3 Electromagnetic compatibility design

Electromagnetic compatibility design is very important for RF frequency source , the design is often the key factor for the success or failure of the RF frequency source design.

The RF circuit is different from the low frequency circuit, the key point of the design is to consider the radiation interference problem. Because the RF circuit is a distributed parameter circuit, a variety of high frequency signals will produce skin effect and coupling effect when operating, resulting in parasitic frequency and other interference signals. This system mainly conducts the electromagnetic compatibility design from the aspects of PCB design , grounding design and shield design.

1) PCB board is the carrier of integrated RF device so reasonable design is very important. Its layout principle is that the RF path is the shortest, which can be achieved by adjusting the direction and position of the device. Effective isolation of high/low frequency signals, input/output signals, high/low power units and key parts are also necessary.

2) Grounding design is a necessary condition for electromagnetic compatibility design . It is usually necessary to ensure that the signal is grounded with small impedance. In this paper, the circuit board is designed as a four-layer board, in which the second and third layers are ground layers, which can suppress noise and reduce interference.

3) RF circuit design needs to consider coupling interference, which is usually completed by shielding signals. The PLL designed in this paper adopts the form of shell packaging. The frequency doubling filter circuit is shielded by the aluminum gold box , and the whole is encapsulated by the aluminum gold box .

4. Performance Analysis

4.1 Phase Noise Analysis

According to PLL theory, the optimal loop bandwidth is determined by the phase noise index of the crystal oscillator and VCO. The phase noise index of 100MHz crystal oscillator is -130dBc/Hz@1kHz, -140dBc/Hz@10kHz. Since the output frequency is 14.2GHz and 50MHz is used as the phase detection frequency, the phase noise of the crystal oscillator in the bandwidth deteriorates by 20log(14200/50)=49dB, and the indexes after deterioration are-81dBc/Hz@1kHz, -91dBc/Hz@10kHz. The indexes of VCO phase noise are: -60dBc/Hz@1kHz, -90dBc/Hz@10kHz, -110dBc/Hz@100kHz. By selecting the appropriate loop bandwidth, the phase noise index can by optimized. The phase noise in the bandwidth can be estimated by the following equation.

PN=PNtot+10logFpfd+20logN

Among which PN is the phase noise in the loop, PNtot is the normalized phase noise of the phase detector, Fpfd is the phase frequency and N is the frequency division ratio.

According to the above analysis and calculation, PN=-223+10log(50×106)+20log(14200/50)=-96dBc/Hz@10kHz. In practical application, the deterioration caused by the circuit to the phase noise is 5dB, and finally the phase noise of the local oscillator signal can reach -90dBc/Hz@10kHz. The phase-locked loop filter circuit is shown in FIG.5. The phase noise of the phase-locked loop is simulated by ADIsimPll software, and the simulation result is -90.3dBc/Hz@10kHz, as shown in Figure 6.

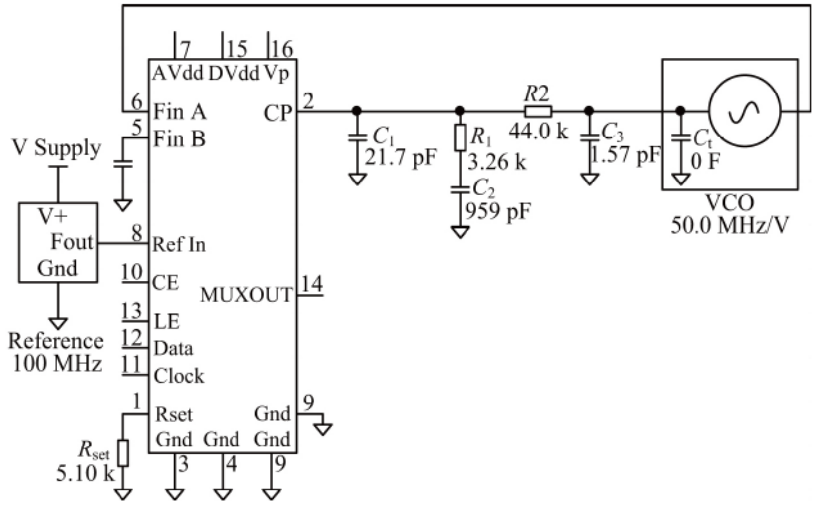

FIG. 5 The phase-locked loop filter circuit

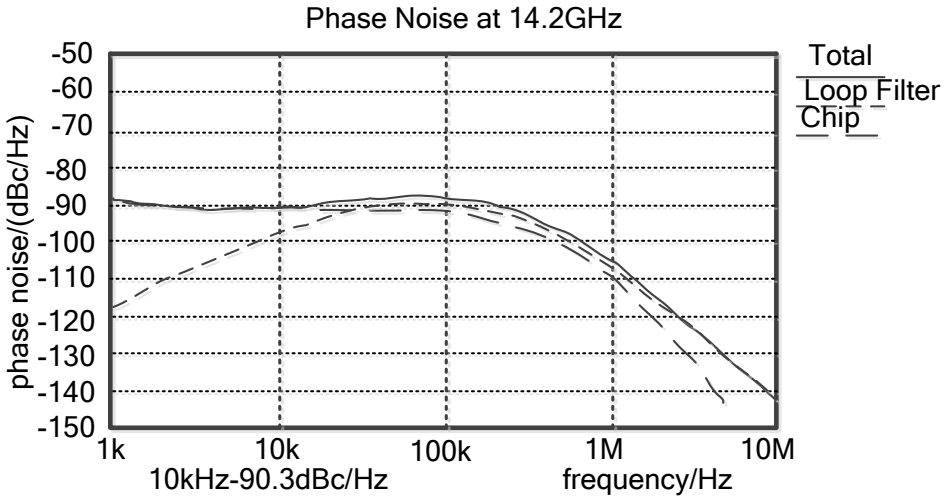

FIG. 6 simulation results of phase noise of phase-locked source in small steps

After frequency doubling, the phase noise deteriorates by about 6dB, so the final phase noise is about-85dBc/Hz@10kHz, which can meet the requirements of the index.

4.2 Stray analysis

Various spurts will be produced in the PLL circuit due to nonlinearity of the device, RF ,radiation and other reasons. The spurt plays a dominant role in the high-frequency circuit designed in this paper, which is caused by the mismatch of the charge pump of the phase detector and can be filtered out when the loop filtering bandwidth is lower than 1/10 of the phase detection frequency.

The stray caused by other reasons can be filtered out by filter to remove the stray outside the bandwidth, and the stray can be suppressed by cavity shielding, signal isolation and power filtering.

In circuit design, the compact layout of PCB components and reasonable wiring between components can also effectively suppress stray.

5. Test Results

5.1 Phase noise test results

The phase noise test result of the final output signal at 10 kHz deviation from the main frequency is shown in FIG. 7.

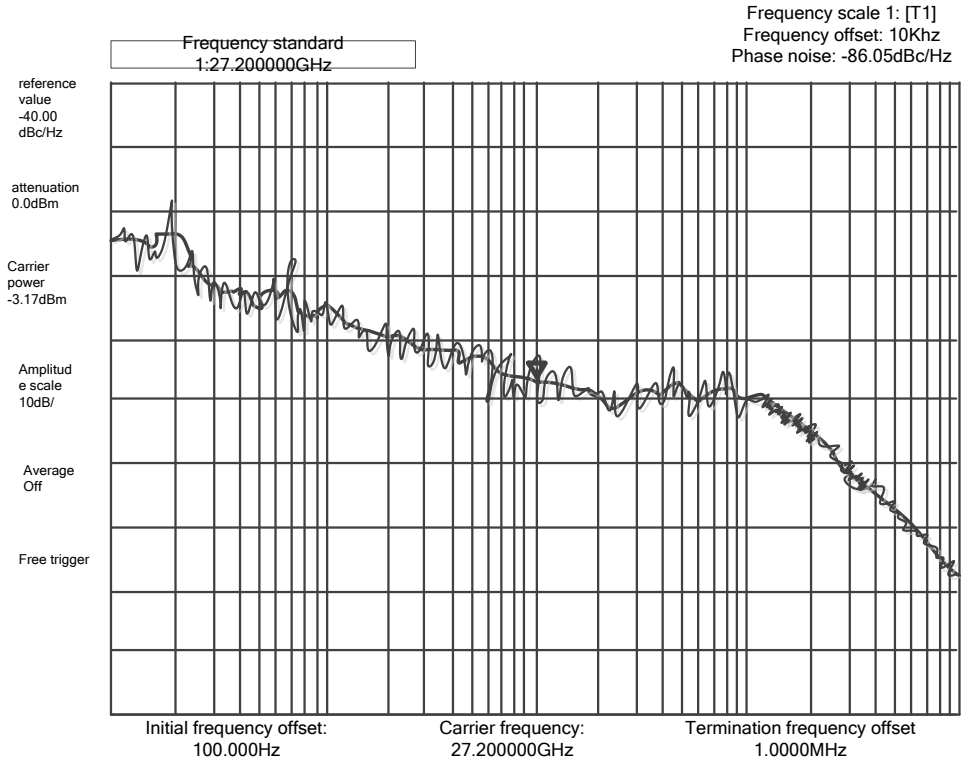

FIG. 7 Phase noise test result of output signal

As can be seen from Figure 7, the measured phase noise of the final output signal is -86.05dBc/Hz@10kHz, which is 1dB different from the theoretical calculation result. So it can be seen that the phase noise of the beacon machine in the actual work is not significantly worse than the theoretical calculation results and simulation results, that is to say, through good circuit shielding and filter optimization, the influence of the thermal noise and power noise of resistance and capacitance components is effectively overcome, and a good effect has been achieved.

5.2 Test results of spurious suppression

The spurious test result of the final output signal is shown in Figure 8. It can be seen from FIG. 8 that the output signal power is -3.2dBm and the spurt suppression is around 73dB, which indicates that the electromagnetic compatibility of each unit circuit is well designed without cross-talk, the device is properly selected, and the filtering effect after frequency multiplication is better.

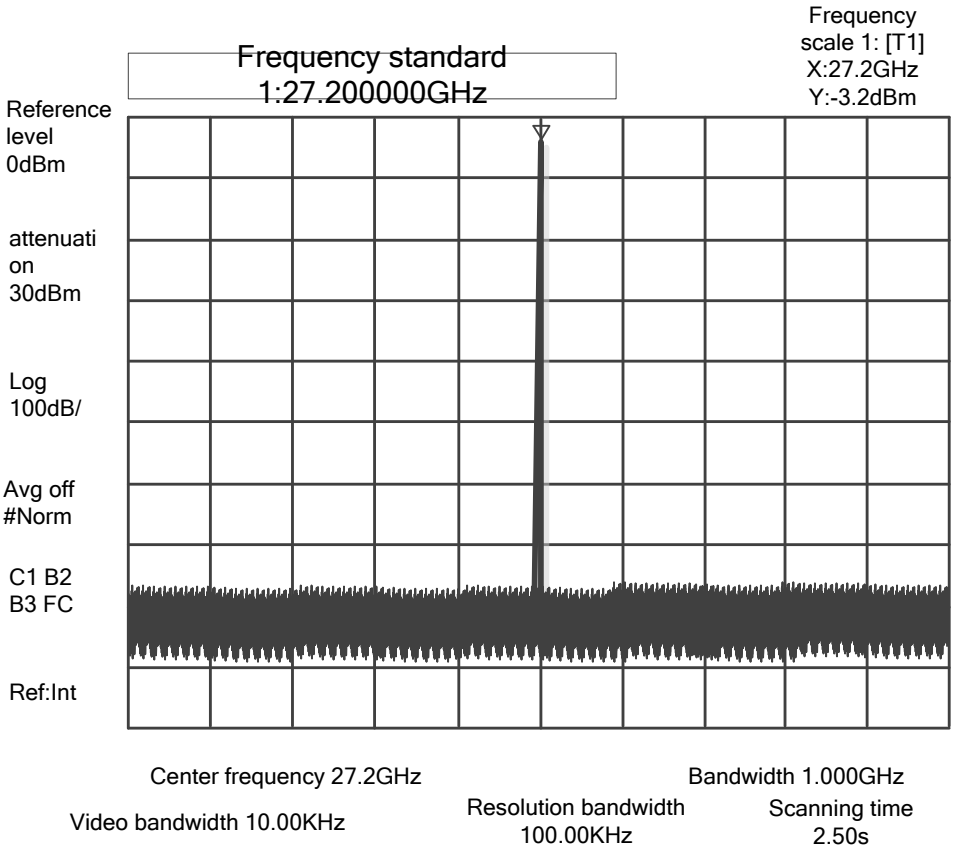

FIG. 8 Results of spurious suppression test

6. Conclusion

In order to meet the needs of system calibration, this paper realizes the signal output with low phase noise, high spurt suppression and small step through reasonable scheme design, using high-performance components, good circuit design and electromagnetic compatibility design, and using phase-locked frequency double filtering. The output frequency is changed by controlling the frequency division coefficient of the phase discriminator, and then the output frequency is extended to Ka-band by double frequency, and the stray is filtered out by loop filter to the maximum extent so the performance index of the beacon machine is improved. The test results show that the test results of phase noise are basically consistent with the theoretical values, which reflects the rationality and scientificity of the design scheme. In the future, VCO voltage presetting and DDS technology need to be further explored to make the frequency source with lower phase noise, wider broadband and smaller step forward so as to meet the needs of the development of electronic equipment.

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