# A Novel Modulation Strategy for Controllable Current Source Converter

Longlong Chen<sup>1, a,\*</sup>, Chong Gao<sup>1</sup>, Taosha Jiang<sup>2, b</sup>, and Sheng Zhang<sup>1</sup>

<sup>1</sup> State Grid Smart Grid Research Institute Co., Ltd. China;

<sup>2</sup> Beijing Huairou Laboratory, China.

<sup>a,\*</sup> chenlong\_003@163.com, <sup>b</sup> jiangtaosha@hrl.ac.cn

**Abstract.** Controllable current source converter (CSC) technology is an effective solution in addressing commutation failure issues. Modulation strategy is the fundamental approach for controlling the valve arm of the converter. Higher switching frequencies result in lower AC harmonics but increased losses in the commutation valve. Lower switching frequencies lead to reduced losses but higher harmonics. The major challenge in engineering currently lies in eliminating the direct conduction state of the valve arms in the current source converter and effectively suppressing harmonics. This paper first analyzes the valve arm signal allocation method in the CSC and examines the mechanism and impact of direct conduction. Then, based on double Fourier signal analysis theory, a SPWM modulation method utilizing the odd multiples of "150Hz" is proposed. Modulation range and signal synchronization methods are analyzed. The effectiveness of the method in terms of duty cycle, transmission characteristics, and saturation characteristics is analyzed. Finally, a comparison is made between this method and traditional linear modulation and asymmetric modulation methods.

Keywords: Controllable Current Source Converter; Modulation method; Operation characteristics.

### 1. Introduction

The standard modulation strategy for Current Source Converter (CSC) is based on Pulse Width Modulation (PWM) techniques. These include the Sinusoidal PWM (SPWM), the Trapezoidal PWM (TPWM), the Space Vector PWM (SV-PWM), and Selected Harmonic Elimination PWM (SHE-PWM).

SPWM is an online modulation approach that generates a sequence of trigger pulses by comparing a high-frequency triangular wave with a reference wave <sup>[1]</sup>. SPWM has the benefits of rapid dynamic response and straightforward implementation. The generated SPWM pulses can accurately reproduce the basic information of the reference wave <sup>[2]</sup>. To reduce the switching loss of the device, the carrier frequency should not be too high, but the generated harmonics are more, and extra filters need to be configured <sup>[3]</sup>.

Trapezoidal Pulse Width Modulation (TPWM) can improve the modulation ratio, therefore is suitable for applications with fixed modulation indices. Its typical modulation range is 0.9~1.05, with a relatively small range of modulation changes <sup>[4]</sup>. TPWM does not improve harmonic suppression.

Under the SV-PWM modulation strategy, the DC current utilization increases, and switching losses decrease. This technique can be efficiently implemented via a digital signal processor, but it requires careful management of redundant vectors' timing to minimize the number of switching. The overall timing control is relatively complex, making it challenging to promote to high voltage levels, and there are also a considerable amount of more low-order harmonics on the AC side. In order to reduce harmonics, a staggered sampling strategy is proposed in reference <sup>[5]</sup>, by offsetting multiple sampling times to offset low-order harmonics.

SHE-PWM is modulation method operates at a low switching frequency. This method can modulate the switching angle to eliminate specific harmonics <sup>[6]</sup>. Despite its advantages, such as low switching frequency, minimal device loss, and favorable low-order AC current harmonic characteristics, it relies on a lookup table for output pulse generation <sup>[7]</sup>. This method is complex,

requires extensive pre-stored data [8], and offers less flexibility compared to TPWM and SPWM, making it suitable for low-switching frequency applications.

The CSC discussed in this paper applies a similar topology presented in reference <sup>[1,9]</sup>. Instead of IGBTs and diodes in the bridge arm, a series of RB-IGCTs are used, as shown in Fig. 1. For simplicity, S1~S6 represent the six converter valve arms, denoting the sequence of bridge arm conduction. The AC side of the CSC has an L-C low-pass filter, capable of filtering out harmonics generated by the converter while supporting the phase shift of the bridge arm current.



In Fig. 1,  $L_{dc}$  represents DC reactance, C represents the commutation capacitor, L is the filter inductance,  $L_{bt}$   $\pi L_{ct}$  signify the stray inductances of the bridge arm and converter branch.  $u_{dc}$  is dc voltage,  $i_{dc}$  is dc current,  $i_{ga}$ ,  $i_{gb}$ , and  $i_{gc}$  are ac curents,  $u_{ga}$ ,  $u_{gb}$ , and  $u_{gc}$  are ac voltages,  $u_{ca}$ ,  $u_{cb}$ , and  $u_{cc}$ are capacitor voltages,  $i_{pa}$ ,  $i_{pb}$ , and  $i_{pc}$  are currents in the outputs of the converter.

# 2. Proposed Modulation Strategy

#### 2.1 Modulation Assignment

Three phase Voltage Source Converter with PWM modulation requires that either the upper or lower valve arm is switched on and can't be simultaneously turned on or off. This operation is explained through a binary switch function, p, detailed as follows

 $p = \begin{cases} 1, \text{ upper valve arm conducting, lower valve arm blocking} \\ -1, \text{ lower valve arm conducting, upper valve arm blocking} \end{cases}$ (1)

In the case of three-phase CSC, a current pathway on the DC side is necessary. At any given time, one of the bridge arms - either upper or lower - is conductive, except at the moment of phase commutation. There is no circumstance in which two upper or two lower bridge arms are conductive simultaneously. Based on their operational conditions, a tri-state switching function is defined as follows:

[1, upper valve arm conducting, lower valve arm blocking

 $S_x = \begin{cases} 0, \text{ upper valve arm and lower valve arm conducting and blocking simultaneously} \\ -1, \text{ upper valve arm blocking, lower valve arm conducting} \end{cases}$ 

(2)

Binary switch functions can be created through the modulation of sine and triangular waves. However, it is not possible to directly generate a tri-state switching function, this must be derived ISSN:2790-1688

Volume-6-(2023)

indirectly by converting the binary logic. The conversion between binary and ternary logic can be done according to formula (3)

$$\begin{bmatrix} S_{a} \\ S_{b} \\ S_{c} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} p_{a} \\ p_{b} \\ p_{c} \end{bmatrix}$$
(3)

To put PWM control into action, the tri-state switching function must satisfy  $S_a + S_b + S_c = 0$ . This leads to nine potential switching combination states for the operation of the converter, six of which are "non-zero level" switching combinations and three are "zero switching combination" states. The associations between the binary and ternary logic states and the switching device are precisely illustrated in Table1.

1	Binary logic			Tri-state logic			Conducting Volvo	
	pa	pb	pc	Sa	Sb	Sc	Conducting valve	
1#	1	1	-1	0	1	-1	S3	S2
2#	1	-1	1	1	-1	0	S1	S6
3#	1	-1	-1	1	0	-1	S1	S2
4#	-1	1	1	-1	0	1	S5	S4
5#	-1	1	-1	-1	1	0	S3	S4
6#	-1	-1	1	0	-1	1	S5	S6
7#	-1	-1	-1	0	0	0	S1	S4
8#				0	0	0	S3	S6
9#	1	1	1	0	0	0	S5	S2

Table 1. CSC arm valve operation status after two-three transformation

In Table 1, states 7# to 9# present a "zero logic combination" issue. These states correspond to a situation in any phase A, B, or C where both the upper and lower arms are conducting. This condition causes short circuit and leads to an instantaneous drop in the valve's DC output voltage. Therefore, removing the zero state of the valve arm switch combination is crucial in resolving the short circuit issue.

#### **2.2 Modulation Signals**

Given the gate driver energy required and the losses generated by the RB-IGCT, the switching signal frequency of the valve arm should not be too high. The proposed approach is as follows:

Initially, a bipolar synchronous modulation strategy is employed to create a binary switching logic based on the amplitude relationship between the sinusoidal modulation wave and the triangular wave. Next, opt for modulation ratios that result in a lower valve voltage by comparing various carrier frequencies. Subsequently, by analyzing the impact of diverse carrier phase and modulation wave phase differences on two-valued logic switching signals, a symmetrical two-valued switch is selected to reduce harmonics generation. Lastly, check and eliminate possibilities for the valve's upper arm and lower arm to short circuit.

To accomplish linear control of the ratio between the triangular wave and the carrier frequency, it is necessary to constrain the initial phases of the carrier and modulation waves, ensuring that the phase difference between the two is zero. Using twice and three times the frequency of 150Hz as examples, the optimal method for carrier comparison is illustrated in Fig. 2.



Fig. 2 Synchronous overmodulation and comparison between 450Hz and 300Hz

Fig. 2 represents a notable difference in the binary switch functions created at carrier frequencies of 450Hz and 300Hz. At 300Hz, the binary switch function loses its symmetry, while the tri-state switch function at 450Hz preserves a good level of symmetry. Likewise, introducing carrier frequencies as multiples of 150Hz will have similar issues. This type of modulation approach is identified as an asymmetric modulation strategy. Such an asymmetric structure disperses the harmonic characteristics of the current, creating ambiguity in the foundation for designing filter parameters. Hence, choosing a carrier frequency that is an odd multiple is considered optimal.

## 3. Simulation and Validation

A simulation of the proposed modulation strategy was simulated on the 250 kV/750 MW CSC system, and the waveforms of the converter's direct voltage and current are shown in Fig. 3. As seen from Fig. 3, during the conversion phase, the presence of stray inductance causes each phase change in the converter to generate a certain amount of overshoot. This could generate a higher continuous overvoltage at large firing angle with the overshoot from capacitance, which needs to be clamped. After system reaches steady state, optimizing the system's operating conditions and adjusting the commutation timing can minimize the overvoltage as low as approximately 1.164 times the direct current voltage.



Fig. 3 Waveform of dc voltage of converter valve

The voltage waveform of the valve arm during steady state is shown in Fig. 4. The voltage waveform is relatively smooth, and the reverse voltage on the valve is only 0.48 times the DC voltage.



Fig. 4 Waveform of voltage of converter arm

The symmetric low-frequency carrier over-modulation method discussed in this paper is compared with linear modulation (with modulation ratio less than 1) in Fig. 5.

As demonstrated in Fig. 5(a), given the same AC voltage, the proposed over-modulation method can achieve a higher DC voltage. Traditional linear modulation converges faster but only achieve a DC voltage of 417kV, failing to meet the requirement of a 500kV rated DC voltage.

Harmonic content is shown in Fig. 5 (b). The symmetric modulation generates a total harmonic content of 45.2%, with the largest harmonic being the 11th, accounting for approximately 27% of the fundamental component. Linear full modulation produces a total harmonic content of 61.1%, with the largest sub-harmonic being the 7th, accounting for approximately 32% of the fundamental component. For high-order harmonics, the harmonic content produced by linear full modulation is also higher than the over-modulation method, but the 5th and 13th harmonic content is significantly lower than the other two methods.

When comparing the strategies for valve arm voltage and current as shown in Fig. 5(c), the linear modulation strategy leads to the highest number of valve voltage switches and has the largest fluctuation amplitude at 270kV. The asymmetric modulation strategy results in a valve voltage of 175kV, while the symmetric modulation strategy exhibits the smallest fluctuation in valve voltage, reducing it to 110kV.

Finally, as shown in Fig. 5(d), nonlinear modulation presents a narrower pulse width, giving the IGCT devices only 0.2 ms to charge gate driver. Linear modulation increases the switch count to 9 times, resulting in elevated switching losses.





(b) Harmonics of valve AC side current under different modulation strategies



different modulation strategies

different modulation strategies

Fig. 5 Comparison between the proposed strategy and traditional strategy technology

## 4. Summary

Based on the SPWM over-modulation strategy, harmonic content was extracted from the converter. For a six-pulse single converter, the AC side contains characteristic harmonics of 5,7,11,13... and so on, while the DC side presents harmonics of 6,12,18,24... and so on. By cascading converters, the harmonic numbers of the AC side of a twelve-pulse converter will increase to 11,13,23,25... etc., and the DC side harmonics will also rise to 12,24,36... and so on.

The DC voltage of the linear SPWM modulation strategy can only reach 80% of the rated parameters. The proposed signal symmetric modulation method and asymmetric modulation method can increase the voltage utilization rate to 100%, but the voltage overshoot of the asymmetric modulation method is higher. The range of valve voltage fluctuation of the linear modulation method is the highest at 270kV, 175kV for the asymmetric strategy, and the symmetric modulation method can reduce it to 110kV.

The harmonics of the three modulation methods are mainly concentrated on 5,7,11... etc. The total harmonic content produced by the asymmetric modulation method is 34.8%, with the largest harmonics being 5 and 7, accounting for about 17% of the fundamental component. The total harmonic content produced by the symmetric modulation method is 45.2%, with the largest harmonic being the 11th, accounting for about 27% of the fundamental component. The total harmonic content produced by the linear full modulation method is 61.1%, with the largest harmonic being the 7th, accounting for about 32% of the fundamental component. By designing a reasonable L-C filtering circuit cut-off frequency and choosing the ratio of AC high-order harmonics to filter resonance frequency to be 2-4, the AC harmonic content can be reduced to below 0.3%, meeting the requirements for ac grid connection.

# Acknowledgments

This work is supported by SGCC project (Research and Development of Controllable Switching Based Current Source Converter, No.5500-202058059A-0-0-00).

# References

- [1] B.Xia, Y.Li, Z.Li, et al.Dual phase shift PWM-CSC based hybrid hvdc transmission system[C], 2018 IEEE 27th International Symposium on Industrial Electronics (ISIE), Cairns, QLD, 2018:378-383.
- [2] E.Giraldo, A.Garces. An adaptive control strategy for a wind energy conversion system based on PWM-CSC and PMSG[J]. IEEE Transactions on Power Systems, 2014, 29(3): 1446-1453.

ISSN:2790-1688

- [3] R.E.Torresolguin, A.Garces, M.Molinas, et al.Integration of offshore wind farm using a hybrid HVDC transmission composed by the PWM current-source converter and line-commutated converter[J].IEEE Transactions on Energy Conversion, 2014,28(1):125-134.
- [4] D.Xu, B.Wu. Multilevel current source inverters with phase shifted trapezoidal PWM[C].2005 IEEE 36th Power Electronics Specialists Conference. Recife, Brazil. IEEE, 2005: 2540-2546.
- [5] Y.Li, B.Wu, D.Xu, et al. Space vector sequence investigation and synchronization methods for active front-end rectifiers in high-power current-source drivers[J]. IEEE Transactions on Industrial Electronics, 2008, 55(3): 1022-1034.
- [6] J.I. Guzman, J. R. Espinoza, L. A. Moran, et al.Selective harmonic elimination in multi-module three-phase current-source converters[J].IEEE Transactions on Power Electronics,2010,25(1):44-53.
- [7] L.Wang, W.Yong.Multilevel current source converter based on SHEPWM[C]. International Conference on Electrical Machines and Systems, ICEMS 2008.Wuhan: ICEMS 2008, 2008:1905-1908.
- [8] J.I.Guzman, P.E.Melin, J.R.Espinoza, et al.Digital implementation of selective harmonic elimination techniques in modular current source rectifiers[J].IEEE Transactions on Industrial Informatics,2013,9(2):1167-1177.
- [9] Z. Bai, Z. Zhang, Y. Zhang. A generalized three-phase multilevel current source inverter with carrier phase-shifted SPWM[C]. 2007 IEEE Power Electronics Specialists Conference. IEEE, 2007: 2055-2060.